REMARKS

The original claims 1-23 have been cancelled, and replaced with claims 24-49 to ensure that the Applicants set forth with particularity what the Applicants regard as their invention.

Also, various typographical errors in the specification have been corrected to secure correspondence between the specification, the figures, and the claims.

Finally, modifications which exemplify subject matter previously described have been added for clarification purposes, as readily contemplated by a person with ordinary skill in the art.

Respectfully submitted,

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John T. Peoples (Reg. No. 28,250)
14 Blue Jay Ct.
Warren, NJ 07059

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Page 9, line 17 has been amended as follows: -- theses system aspects.--.

Page 215, line 1, after "super-stage." the following has been added --Note that if $\gamma(p) = \gamma(q)$ in the guide of the network, where $p<q$, the q-th symbol of the routing tag $Q_{\gamma(q)}$ will repeat the p-th symbol $Q_{\gamma(p)}$, when $Q_{\gamma(p)} = Q_{\gamma(q)}$ = 'bicast', the packet may be bicasted at stage-p and then be bicasted again at stage-q such that undesired extra copies of the packet will be produced. Therefore, whenever $\gamma(p) = \gamma(q)$ in the guide of the network, the bicasting function of the whole stage of switching nodes at either stage-p or stage-q should be disabled to prevent such situation.--.

Page 218, line 5 has been amended as follows: --cells.--.

Page 221, line 9 has been amended as follows: --surface 7407 of a rectangular interface boards, and the output switching elements are--.

Page 222, line 2 has been amended as follows: --realization of ~~an~~ "fiber-array package". Each I/O switching element in a fiber-array--.

Page 223, added after line 1:--Once a PCB is resulted from a step of PCB implementation, it cannot be used in another step of PCB implementation, and the same for the IC chip.--.

Page 224, line 9 has been amended as follows: --construction and ~~cannot be~~ is not implemented in any of the aforementioned levels. Such a--.

Page 233, line 9 has been amended as follows: --node by 2^d lines. In this case, $D=2^d$ where D is the scale-down factor. The parameter d is called the "scale-down exponent".--.

Page 233, line 17 has been amended as follows: --2^{n-r} $2^r \times 2^r$ ~~input~~ output nodes, the interstage exchange is induced by a permutation σ on integers--.

Page 234, lines 17-18 have been amended as follows: --r+1–d to 1, r+2–d to 2, ... , n–2d to n–r–d, and hence the interstage exchange is the 2^d-line version of the $(r-d)^{th}$ power of the $2^{n-2d} \times 2^{n-2d}$ shuffle exchange $SHUF^{(n-2d)}$. This is referred to as the "default choice" for π in this context.--.

Page 235, line 2 has been amended as follows: --2^d-line version of the exchange $SWAP^{(n-2d,\, r-d)}$.--.

Page 235, line 14 has been amended as follows: --employ the modified 2-stage interconnection, the resulting network is not a ~~$2^n \times 2^n$ n-stage~~ --.

Page 236, lines 2-3 have been amended as follows: --essence, when one or more of the recursive steps in the recursive application of ~~the modified~~ bit-permuting 2-stage interconnection employ the modified 2-stage interconnection, the resulting network is ~~creates~~ routable ~~bit-permuting networks~~. Therefore, the self-routing mechanism for the--.

Page 236, lines 14-16 have been amended as follows: --routing tag $D_{\gamma(p)}$ is equal to the q-th symbol $D_{\gamma(q)}$, where $p<q$, the whole stage of switching nodes at either stage-p or stage-q can be disabled~~, or alternatively, simply treat the switching at stage p as superfluous~~.--.

Page 237, lines 6-7 have been amended as follows: --routing tag are distinct. ~~Alternatively, the switching performed in the 1st and 3rd stages is superfluous.~~--.

Page 240, lines 11-12 have been amended as follows: --Therefore, when applying the modified 2-stage interconnection, there are ~~d~~ D units of interconnection lines between

any pair of input node and output node, where D is the scale-down factor, so this arrangement--.

Page 240, lines 17-18 have been amended as follows: -- one way to accommodate this is to add a small adaptor to each ~~d~~ D units of lines of each input node and each output node. This method is especially convenient when ~~d~~ D is not too large--.

Page 241, line 1 has been amended as follows: --and the ~~d~~ D units of lines connecting each pair of input node and output node are neighboring--.

Page 241, line 2 has been amended as follows: --to each other. The following is such an example with ~~d=1~~D=2. FIG. 79A is the planar--.

Page 241, lines 5-6 have been amended as follows: --respectively represent an 8-unit-in-8-unit-out PCB, and as ~~d=1~~D=2, each input node is connected to each output node by ~~$2^d=2^1=$~~2 units of interconnection lines (**7903**), resulting--.

Page 242, line 15 has been amended as follows: --each of the input switching nodes and/or an input exchange should be prepended to each of--.

Page 243, line 13 has been amended as follows: --regarded as a special kind of the ~~interface-board-packaging~~ interface-board packaging.--.